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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:
Daren Allee

Serial No.: 09/400,508

Filed: 9/20/99

For: LOW NOISE LOGIC GATE

Group Art Unit: 2819

Examiner: J. Cho

Atty. Dkt. No.: 2069.002296/TT2275/TDKM

APPEAL BRIEF

BOX AF
Assistant Commissioner of Patents
Washington, D.C. 20231

Sir:

Applicant hereby submits an original and two copies of this Appeal Brief to the Board of Patent Appeals and Interferences in response to the final Office Action dated August 13, 2001. The Notice of Appeal was timely filed on November 15, 2001, along with a one month extension of time. The due date for this Appeal Brief was January 15, 2002.

Also, a request for a one month extension of time to respond is included herewith. This one month extension will bring the due date to February 15, 2002. The extension fee of $110.00 is included in the attached check.

The fee for filing this Appeal Brief is $320, and is attached hereto. Should such request or fee be deficient or absent, consider this paragraph such a request and authorization to withdraw the appropriate fee.

If the check is inadvertently omitted, or should any additional fees under 37 C.F.R. §§ 1.16 to 1.21 be required for any reason relating to the enclosed material, or should an overpayment be included herein, the Assistant Commissioner is authorized to deduct or credit said fees from or to William, Morgan & Amerson, P.C.'s Deposit Account No. 50-0786 /2069.002200.

I. REAL PARTY IN INTEREST

The prosecution history reveals that the present application was initially assigned to Advanced Micro Devices, Inc. in an assignment document filed with the original application and recorded at Reel 010260, Frame 0886. Advanced Micro Devices, Inc. subsequently assigned the present application to Legerity, Inc. in an assignment document recorded at Reel 011700, Frame 0686. The real party in interest is Legerity, Inc.

II. RELATED APPEALS AND INTERFERENCES

Applicant is unaware of any related appeals or interferences that might affect the outcome of this proceeding.

Applicant directs the Board's attention to the following related patents:

U.S. Patent No. 6,236,280, filed September 20, 1999, entitled "Low-Noise Voltage Controlled Oscillator," whose inventor is Daren Allee (Atty. Dkt No. 2069.002100/TT2272); and

U.S. Patent No. 6,208,125, filed September 20, 1999, entitled "Low-Noise Current Source," whose inventor is Daren Allee (Atty. Dkt. No. 2069.002300/TT2274.

III. STATUS OF THE CLAIMS

Claims 1-16 are pending in the present application. The Office Action dated August 13, 2001 finally rejected each of claims 1-16. More particularly:

- Claim 1 was rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Letter Patent No. 6,078,194 ("*Lee*");
- Claim 2 was rejected under 35 U.S.C. § 103(a) as being unpatentable over *Lee*.
- Claim 3 was rejected under 35 U.S.C. § 103(a) as being unpatentable over *Lee* in view of U.S. Letters Patent No. 5,955,893 ("*Chang et al.*");
- Claim 4 was rejected under 35 U.S.C. § 103(a) as being unpatentable over *Lee* in view of U.S. Letters Patent No. 3,651,334 ("*Thompson et al.*");
- Claim 5 was rejected under 35 U.S.C. § 103(a) as being unpatentable over *Lee* in view of U.S. Letters Patent No. 5,602,494 ("*Sunstrom*");
- Claim 16 was rejected under 35 U.S.C. § 103(a) as being unpatentable over modified (sic) *Lee*; and
- Claims 6-15 were rejected with the statement, "Apparatus claims 6-15 are essentially the same in scope as rejected apparatus claims 1-5 and 16 and are rejected similarly."

Applicant has appealed each of the rejections of claims 1-16.

IV. STATUS OF AMENDMENTS

There were no amendments after the final rejection of August 13, 2001.

V. SUMMARY OF THE INVENTION

The invention is directed to a logic gate capable of providing an output that is responsive to a first control input but is not substantially affected by voltage changes in the power supplied to the logic gate. Supply voltages are well known to vary about the desired value due to power plane droop and other reasons. A control input, such as the first control input over the terminal (32), typically tracks the variations in the supply voltage, *i.e.*, as the supply voltage rises, the input value of the control input rises and as the supply voltage falls, the input value of the control input falls. These changes are separate and different from any designed or intended changes in the input value of the control input.

FIGURE 2

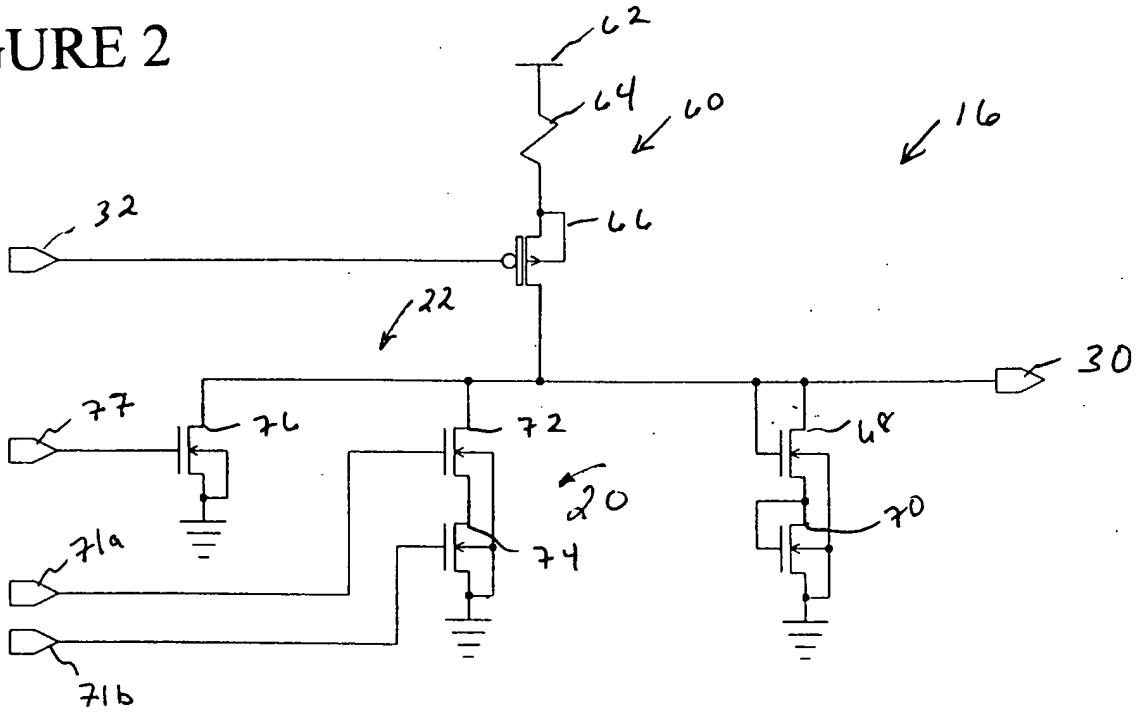


Figure A - FIGURE 2 of Pending Application

More particularly, referring to FIGURE 2 (reproduced here as Fig. A), the illustrated embodiment of the invention includes a low noise current source (60) coupled to a power supply (62). The gate of the transistor (66) is coupled to the control input terminal (32), such that an

analog voltage placed on the control input terminal (32) affects the magnitude of the current supplied.

The AND gate (20) of the comparator circuit (16) is formed by a pair of transistors (72, 74) serially coupled between the complementary phase output terminal (30) and system ground. The gates of the transistors (72, 74) are coupled to the output terminals (71a, 71b) of the edge delay circuit (12; shown in FIGURE 1 not included here) and the NOR gate (34). Thus, when the gates of the transistors (72, 74) are both logically high, they both conduct current, pulling the complementary phase output terminal (30) toward system ground. When neither, or only one, of the gates of the transistors (72, 74) are logically high, then the current source (60) supplies current to charge the complementary output terminal (30). [Application pp. 7, l. 20 – p. 8, l. 14]

VI. ISSUES ON APPEAL

A. Whether claim 1 is anticipated under 35 U.S.C. § 102(e) by *Lee*.

B. Whether claims 2-16 are obvious under 35 U.S.C. § 103(a) by *Lee* either alone or in combination with assorted secondary references.

VII. GROUPING OF THE CLAIMS

The claims 1-16 rise or fall together.

VIII. ARGUMENT

A. Applicable Legal Standards

1. Anticipation

"It is by now well settled that the burden of establishing a *prima facie* case of anticipation resides with the Patent and Trademark Office. *In re Piasecki*, 745 F.2d 1468, 1472, 223 U.S.P.Q. 785, 788 (Fed. Cir. 1984) quoting *In re Warner*, 379 F.2d 1011, 1016, 154 U.S.P.Q.

173, 177 (C.C.P.A. 1967)." *Ex parte Skinner*, 2 U.S.P.Q.2d (BNA) 1788, 1788-89 (Bd. Pat. App. & Int. 1987). An anticipating reference by definition must disclose every limitation of the rejected claim in the same relationship to one another as set forth in the claim. *In re Bond*, 15 U.S.P.Q.2d (BNA) 1566, 1567 (Fed. Cir. 1990). "[I]t is incumbent upon the examiner to identify wherein each and every facet of the claimed invention is disclosed in the applied reference." *Ex parte Levy*, 17 U.S.P.Q.2d (BNA) 1461, 1462 (Pat. & Tm. Off. Bd. Pat. App. & Int. 1990).

2. Obviousness

For a 35 U.S.C. § 103(a) rejection, the factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966) MPEP 804(B)(1). It is the Office's burden to establish *prima facie* that the claimed invention is obvious. This includes the burden of showing that the references are within the scope and content of the prior art. *In re Oetiker*, 24 U.S.P.Q.2d (BNA) 1443, 1445-46 (Fed. Cir. 1992). Where multiple references are cited, this includes the burden of establishing that the references are combinable. *Oetiker*, at 1446.

B. Rejections

1. Anticipation

Applicant's invention is generally directed to a logic gate that is capable of delivering an output signal that has a relatively low noise component. In particular, claim 1 recites:

> 1. A logic gate, comprising:
>
> a low noise current source coupled between a first terminal of a voltage supply and an output terminal, said low noise current source being capable of delivering a preselected voltage signal to said output terminal having a magnitude responsive to a first control signal relatively independent of the magnitude of the voltage on said first terminal of said voltage supply; and

at least one switching element coupled between the output terminal and a second terminal of the voltage supply, said switching element being capable of coupling said output terminal to said second terminal of said voltage supply in response to receiving a control signal

Note the feature of the low noise current source "capable of delivering a preselected voltage signal to said output terminal having a magnitude responsive to a first control signal relatively independent of the magnitude of the voltage on said first terminal of said voltage supply." [Emphasis added.] That is, the output of the current source is relatively free from variations in the voltage level of the voltage supply.

As alluded to above, it is well known in the art that variations in the supply voltage propagate through the system to the control voltages. The control voltages draw power from the power planes. Any variation in voltage on the power planes leads to some variation in the voltage supplied to the control signals. Under these and similar conditions, it should be clear that if the supply voltage droops by 1 volt, then the control signal voltage also droops, by some portion, perhaps all, of the 1 volt. The low noise current source of claim 1 has the feature that the "preselected voltage signal to said output terminal" is "relatively independent" of the "magnitude of the voltage...of the voltage supply." Undesired changes to the input control signal and the power supply typically lead to undesired changes in the output signal, but the present invention moderates or eliminates the effect of those undesired changes.

At least one factor that contributes to the independence of the output of the current source relative to the voltage supply is the use of a p-type transistor (66 or 84) when the voltage supply (62) is a positive voltage. This is the illustrated embodiment shown in FIGURE A herein. Assume for the sake of discussion that the voltage supply (62) is normally at about 5 volts, but

because of noise or other interference, the voltage supply (62) dips to about 4.5 volts. The circuitry providing a control signal to the p-type transistor (66) over the terminal (32) will likewise be reduced since it is also powered by the voltage supply (62). The reduced level of the signal applied to the gate of the p-type transistor (66) causes it to pass more current, thereby maintaining the voltage level of the signal delivered by the current source. While a drop in supply voltage would typically result in a drop in the output signal, the illustrated embodiment of the invention acts to minimize this effect to a reasonable degree.

Lee discloses reduced power logic gates. Specifically, *Lee* purports to show logic gates that draw virtually no power when not in use. [Abstract; col. 6, ll. 57-58]. *Lee* does not teach or fairly suggest controlling noise as with the present invention.

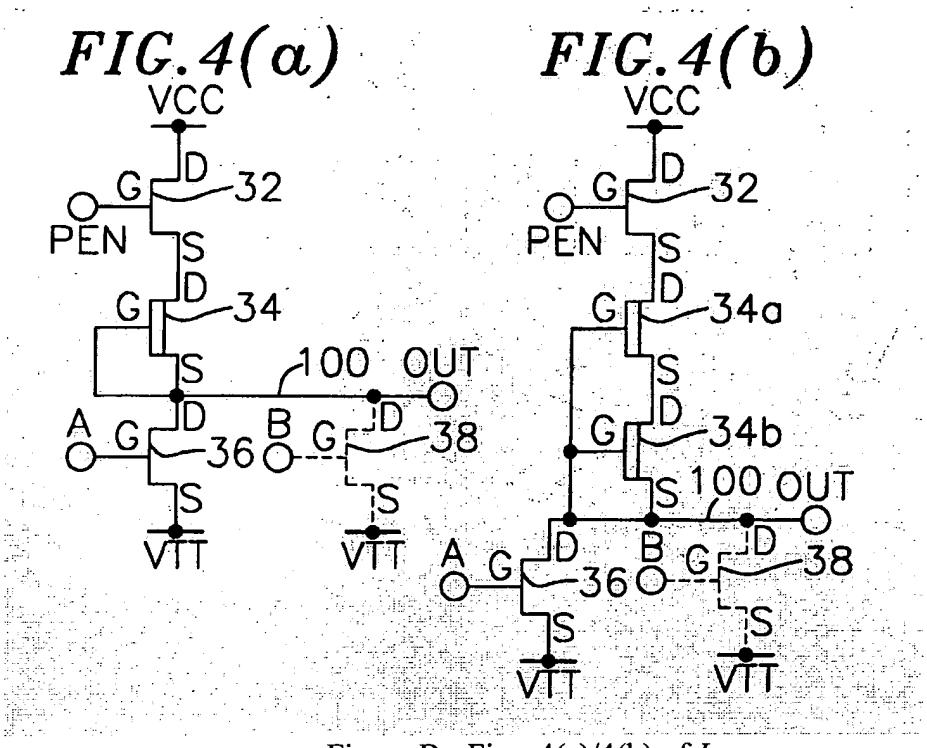


Figure B - Figs. 4(a)/4(b) of *Lee*

As an anticipation rejection must fail if any element of the claim is not shown in the prior art in the manner shown in the claim, we look to *Lee* for a teaching of a low noise current source

that is capable of delivering a preselected voltage signal to its output terminal that has a magnitude responsive to a first control signal relatively independent of the magnitude of the voltage on the first terminal of the voltage supply. Referring to Fig. B showing Figs. 4(a) and 4(b) of *Lee*, as the Examiner has done since the Office Action of September 26, 2000, we note that the transistor (32) of *Lee* is an n-type transistor and the voltage supply Vcc appears to be a positive voltage.

As far as noise in the output signal (OUT 100), even when improperly interpreted in hindsight using to the Applicant's disclosure, *Lee* fails to show all of the elements of claim 1. Looking to the example given above, if the Examiner's interpretation of transistor (32) as a current source is valid, a droop in the power supply voltage Vcc of *Lee* would result in a droop in the PEN voltage of *Lee*, leading to a lower output signal (OUT 100) of *Lee*. Concurrently, the droop in the power supply voltage Vcc of *Lee* would also lead to the lower output signal (OUT 100) of *Lee*. Thus, *Lee* does not teach the element of claim 1 of "delivering a preselected voltage signal to said output terminal having a magnitude responsive to a first control signal relatively independent of the magnitude of the voltage on said first terminal of said voltage supply." *Lee* discloses a transistor (32) with an output voltage that is very dependent on the supply voltage Vcc, both in control signal input (PEN) and how the transistor (32) produces its output based on the supply voltage Vcc.

The Examiner has argued since the First Office Action dated September 26, 2000, that *Lee* could be made to be operate relatively independent if the n-type transistor were replaced with a p-type transistor. Applicant respectfully disagrees with the Examiner's position as discussed below, but even if it were true that *Lee* could be modified to achieve Applicant's invention, the modification would render *Lee* ineffective as an anticipatory reference under 35

U.S.C. § 102. That is, *Lee* clearly does not anticipate claim 1. This distinction was timely brought to the Examiner's attention for the first time in the Response to Office Action Dated September 26, 2000.

2. Obviousness

Further, *Lee* does not render claim 1 obvious. The Examiner's suggestion to replace the n-type transistor (32) of *Lee* with a p-type transistor would render the circuit disclosed in *Lee* inoperable, even assuming that the replacement in *Lee* was taught or fairly suggested by prior art. Clearly, the control signal PEN, shown being delivered to the gate of the n-type transistor (32) of *Lee,* would cause significant misoperation of the circuit disclosed in *Lee* if the transistor (32) was altered to be a p-type transistor. Further, inverting the PEN signal to compensate for the now substituted p-type transistor is illogical. The circuit of Fig. 4(a) of *Lee*, which includes the transistor 32, is an inverter. [col. 6, ll. 26-28] Thus, the modification would necessarily include adding an inverter in front of the modified inverter so that the appropriate output signal could be produced.

Independent claims 6 and 11 also include the feature of the low noise current source being "capable of delivering a preselected voltage signal to said output terminal having a magnitude responsive to a first control signal relatively independent of the magnitude of the voltage on said first terminal of said voltage supply". Thus, all independent claims, 1, 6, and 11, are allowable over *Lee*. Likewise, all dependent claims therefrom are also allowable over *Lee.*

Dependent claims 3, 4, and 5 were rejected over *Lee* in view of another reference, *Chang et al.*, *Thompson et al.*, and *Sunstrom*, respectively. The Examiner has never argued that any of *Chang et al.*, *Thompson et al.*, and *Sunstrom* remove the deficiency of *Lee* described above.

Instead, *Chang et al.*, *Thompson et al.*, and *Sunstrom* have been cited for showing separate single elements, which happen to be elements of the respective claim, along with an obviousness conclusion given without any supporting evidence. *Chang et al.* shows that an intrinsic transistor may be employed in a circuit. *Thompson et al.* shows a capacitor coupled in a circuit. *Sunstrom* shows a diode (see 142 in Fig. 2). Each combination fails to teach or fairly suggest the element of independent claims 1, 6, and 11 of a low noise current source being "capable of delivering a preselected voltage signal to said output terminal having a magnitude responsive to a first control signal relatively independent of the magnitude of the voltage on said first terminal of said voltage supply". Applicant has timely traversed each of these rejections, starting with the Response to Office Action Dated September 26, 2000.

The Examiner characterized claims 6-15 as being essentially the same in scope as rejected apparatus claims 1-5 and 16, and thus rejected claims 6-15 "similarly." Applicant has timely traversed this vague "rejection" for the same reasons discussed above in conjunction with claims 1-5. Further, however, independent claim 6 includes an additional recitation to the current source having an intrinsic transistor. As discussed in Applicant's specification, the use of an intrinsic transistor has further significant benefits in enhancing the independence of the output signal of the logic gate from "noise" appearing on the voltage supply. *Lee* neither discloses nor suggests that an intrinsic transistor could be used in a current source of a logic gate, or that using such an intrinsic transistor may beneficially reduce noise produced by the logic gate. While *Chang et al.* shows that an intrinsic transistor may be employed in a circuit, *Chang et al.* never discusses the use of an intrinsic transistor to reduce noise produced by the logic gate. That is, *Chang et al.* adds nothing to *Lee* to further the Examiner's argument that it would be obvious to replace the n-type transistor of *Lee* with a p-type intrinsic transistor for the purpose of producing

a low noise current source that is capable of delivering a preselected voltage signal to its output terminal that has a magnitude responsive to a first control signal relatively independent of the magnitude of the voltage on the first terminal of the voltage supply. Accordingly, claim 6 and its dependent claims (7-9) are patentably distinct over *Lee* and the remaining applied references. Further, claims 6-15 are also patentably distinct over the prior art for at least the reasons discussed above in conjunction with claim 1.

The Examiner's arguments may be best characterized as hindsight reconstruction along with "obvious to try" the Applicant's invention in light of the cited art. MPEP 2144.06 discusses this situation, in the quote from *In re Geiger*, 815 F.2d 686, 2 USPQ2d 1276 (Fed. Cir. 1987), as not being a winning argument.

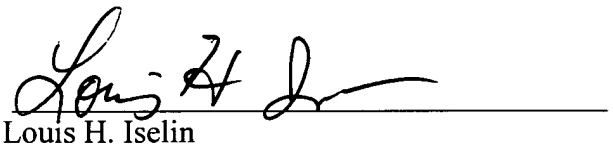
IX. CONCLUSION

Applicant respectfully submits that the rejections were improvident and should be withdrawn because the cited references fail to teach or suggest at least one feature of the claims. In independent claims 1, 6, and 11, this limitation is a low noise current source being "capable of delivering a preselected voltage signal to said output terminal having a magnitude responsive to a first control signal relatively independent of the magnitude of the voltage on said first terminal of said voltage supply". All dependent claims variously also recite these limitations. 35 U.S.C. § 112, ¶ 2. "If the examination at the initial stage does not produce a *prima facie* case of unpatentability, then without more the application is entitled to grant of the patent." *In re Oetiker*, 24 U.S.P.Q.2d (BNA) 1443, 1444 (Fed. Cir. 1992). This application has been through an initial examination and an examination as a Continuing Prosecution Application under 37 CFR § 1.53(d). Applicants therefore respectfully request that rejections be reversed and the claims be allowed to issue.

Finally, claims 2-10 and 12-16 were objected to an inconsequential formality for which the Applicant consents to the proposed correction, which may be entered by Examiner's Amendment.

Please date stamp and return the enclosed postcard to evidence receipt of this document.

Respectfully submitted,



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Date: February 15, 2002

Appendix

1. A logic gate, comprising:

a low noise current source coupled between a first terminal of a voltage supply and an output terminal, said low noise current source being capable of delivering a preselected voltage signal to said output terminal having a magnitude responsive to a first control signal relatively independent of the magnitude of the voltage on said first terminal of said voltage supply; and

at least one switching element coupled between the output terminal and a second terminal of the voltage supply, said switching element being capable of coupling said output terminal to said second terminal of said voltage supply in response to receiving a control signal.

2. A logic gate, as set forth in claim 1, wherein said low noise current source includes a transistor and a resistor serially coupled between the first terminal of the voltage supply and the output terminal, the transistor having a gate capable of receiving the first control signal.

3. A logic gate, as set forth in claim 2, wherein said transistor is an intrinsic transistor.

4. A logic gate, as set forth in claim 1, including a capacitor coupled between the output terminal and the second terminal of the voltage supply.

5. A logic gate, as set forth in claim 1, including at least one clamping diode coupled between the output terminal and the second terminal of the voltage supply.

6. A logic gate, comprising:

a low noise current source coupled between a first terminal of a voltage supply and an output terminal, said low noise current source including an intrinsic transistor being capable of delivering a preselected voltage signal to said output terminal having a magnitude responsive to a first control signal relatively independent of the magnitude of the voltage on said first terminal of said voltage supply; and

at least one switching element coupled between the output terminal and a second terminal of the voltage supply, said switching element being capable of coupling said output terminal to said second terminal of said voltage supply in response to receiving a control signal.

7. A logic gate, as set forth in claim 6, wherein said low noise current source includes a resistor serially coupled with said intrinsic transistor between the first terminal of the voltage supply and the output terminal, the intrinsic transistor having a gate capable of receiving the first control signal.

8. A logic gate, as set forth in claim 6, including a capacitor coupled between the output terminal and the second terminal of the voltage supply.

9. A logic gate, as set forth in claim 6, including at least one clamping diode coupled between the output terminal and the second terminal of the voltage supply.

10. A logic gate, as set forth in claim 6, wherein said intrinsic transistor is a p-type transistor.

11. A logic gate, comprising:

a low noise current source coupled between a first terminal of a voltage supply and an output terminal, said low noise current source including a p-type transistor being capable of delivering a preselected voltage signal to said output terminal having a magnitude responsive to a first control signal relatively independent of the magnitude of the voltage on said first terminal of said voltage supply; and

at least one switching element coupled between the output terminal and a second terminal of the voltage supply, said switching element being capable of coupling said output terminal to said second terminal of said voltage supply in response to receiving a control signal.

12. A logic gate, as set forth in claim 11, wherein said low noise current source includes a resistor serially coupled with the p-type transistor between the first terminal of the voltage supply and the output terminal, the transistor having a gate capable of receiving the first control signal.

13. A logic gate, as set forth in claim 11, wherein said p-type transistor is an intrinsic transistor.

14. A logic gate, as set forth in claim 11, including a capacitor coupled between the output terminal and the second terminal of the voltage supply.

15. A logic gate, as set forth in claim 11, including at least one clamping diode coupled between the output terminal and the second terminal of the voltage supply.

16. A logic gate, as set forth in claim 2, wherein said transistor is a p-type transistor.